CLAIMS

What is claimed is:

1. An operational amplifier for use in a switched capacitor circuit, the operational amplifier comprising:
   a. a grounded source operational amplifier circuit; and
   b. a dynamic current switching circuit coupled to the grounded source operational amplifier circuit,
   wherein the dynamic current switching circuit is configured to reduce power dissipation in the operational amplifier circuit.

2. The operational amplifier according to claim 1, wherein the grounded source operational amplifier circuit includes:
   a. a main amplifier core circuit; and
   b. a biasing circuit.

3. The operational amplifier according to claim 2, further comprising an upper gain enhancement circuit including a first PMOS cascode, a second PMOS cascode and an AUXP operational amplifier, wherein the upper gain enhancement circuit maintains an upper gain bias voltage across a first PMOS current sources and a second PMOS current source.

4. The operational amplifier according to claim 3, wherein the upper gain bias voltage is 500mV.

5. The operational amplifier according to claim 2, further comprising a lower gain enhancement circuit including a first NMOS cascode, a second NMOS cascode and an AUXN operational amplifier, wherein the lower gain enhancement circuit maintains a lower gain bias voltage across a main input pair.

6. The operational amplifier according to claim 5, wherein the lower gain bias voltage is 400mV.

7. The operational amplifier according to claim 2, wherein the dynamic current switching circuit includes:
   a. a main mirror diode;
   b. a main fixed current source;
   c. a first current switch; and
   d. a second current switch.

8. The operational amplifier according to claim 7, further comprising a first main leg and a second main leg in a branch of the main amplifier core circuit, wherein the first main leg and the second main leg are configured such that an input pair bias current and an output pair bias current flow in the branch.

9. The operational amplifier according to claim 8, wherein when the operational amplifier circuit is in a reset state, an input signal is high, and the second current switch directs a reset current through its drain, thereby allowing none of the reset current to flow through the main mirror diode and through each of the first main leg and the second main leg.

10. The operational amplifier according to claim 9, wherein the reset current flowing through each of the first main leg and the second main leg is 250uA.

11. The operational amplifier according to claim 8, wherein when the operational amplifier circuit is in an amplification state, the input signal is low, and the second current switch is off, thereby allowing an amplification current to flow through the main mirrored diode, the first current switch, the second current switch, and each of the first main leg and the second main leg.

12. The operational amplifier according to claim 11, wherein the amplification current flowing through each of the first main leg and the second main leg is 1.2mA.

13. The operational amplifier according to claim 2, wherein a common mode output voltage is set to 1.5V.

14. The operational amplifier according to claim 2, wherein a common mode input voltage is set to 1.1V.

15. An operational amplifier for use in a switched capacitor circuit, the operational amplifier comprising:

a. a main amplifier core circuit including a first main leg and a second main leg in a branch of the main amplifier core circuit, wherein the first main leg and the second main leg are configured such that an input pair bias current and an output pair bias current flow in the branch, further wherein the main amplifier core circuit includes:

i. an upper gain enhancement circuit including a first PMOS cascode, a second PMOS cascode and an AUXP operational amplifier, wherein the upper gain enhancement circuit maintains an upper gain bias voltage across a first PMOS current sources and a second PMOS current source; and

ii. a lower gain enhancement circuit including a first NMOS cascode, a second NMOS cascode and an AUXN operational amplifier, wherein the lower gain enhancement circuit maintains a lower gain bias voltage across a main input pair,

b. a biasing circuit; and

c. a dynamic current switching circuit coupled to the grounded source operational amplifier circuit,

wherein the dynamic current switching circuit is configured to reduce power dissipation in the operational amplifier circuit.

16. The operational amplifier according to claim 15, wherein the upper gain bias voltage is 500mV.

17. The operational amplifier according to claim 15, wherein the lower gain bias voltage is 400mV.

18. The operational amplifier according to claim 15, wherein the dynamic current switching circuit includes:
    a. a main mirror diode;
    b. a main fixed current source;
    c. a first current switch; and
    d. a second current switch.

19. The operational amplifier according to claim 18, wherein when the operational amplifier circuit is in a reset state, an input signal is high, and the second current switch directs a reset current through its drain, thereby allowing none of the reset current to flow through the main mirror diode and through each of the first main leg and the second main leg.

20. The operational amplifier according to claim 19, wherein the reset current flowing through each of the first main leg and the second main leg is 250uA.

21. The operational amplifier according to claim 18, wherein when the operational amplifier circuit is in an amplification state, the input signal is low, and the second current switch is off, thereby allowing an amplification current to flow through the main mirrored diode, the first current switch, the second current switch, and each of the first main leg and the second main leg.

22. The operational amplifier according to claim 21, wherein the amplification current flowing through each of the first main leg and the second main leg is 1.2mA.

23. The operational amplifier according to claim 15, wherein a common mode output voltage is set to 1.5V.

24. The operational amplifier according to claim 15, wherein a common mode input voltage is set to 1.1V.

25. An operational amplifier for use in a switched capacitor circuit, the operational amplifier comprising:
    a. a main amplifier core circuit including a first main leg and a second main leg in a branch of the main amplifier core circuit;
    b. a biasing circuit; and
    c. a dynamic current switching circuit coupled to the grounded source operational amplifier circuit,

wherein the dynamic current switching circuit is configured to reduce power dissipation in the operational amplifier circuit.

26. The operational amplifier according to claim 25, wherein the main amplifier core circuit includes an upper gain enhancement circuit including a first PMOS cascode, a second PMOS cascode and an AUXP operational amplifier, further wherein the upper gain enhancement circuit maintains an upper gain bias voltage across a first PMOS current sources and a second PMOS current source.

27. The operational amplifier according to claim 25, wherein the main amplifier core circuit includes a lower gain enhancement circuit including a first NMOS cascode, a second NMOS cascode and an AUXN operational amplifier, further wherein the lower gain enhancement circuit maintains a lower gain bias voltage across a main input pair.

28. The operational amplifier according to claim 25, wherein the upper gain bias voltage is 500mV.

29. The operational amplifier according to claim 25, wherein the lower gain bias voltage is 400mV.

30. The operational amplifier according to claim 25, wherein the dynamic current switching circuit includes:
    a. a main mirror diode;
    b. a main fixed current source;
    c. a first current switch; and
    d. a second current switch.

31. The operational amplifier according to claim 30, wherein when the operational amplifier circuit is in a reset state, an input signal is high, and the second current switch directs a reset current through its drain, thereby allowing none of the reset current to flow through the main mirror diode and through each of the first main leg and the second main leg.

32. The operational amplifier according to claim 31, wherein the reset current flowing through each of the first main leg and the second main leg is 250uA.

33. The operational amplifier according to claim 30, wherein when the operational amplifier circuit is in an amplification state, the input signal is low, and the second current switch is off, thereby allowing an amplification current to flow through the main mirrored diode, the first current switch, the second current switch, and each of the first main leg and the second main leg.

34. The operational amplifier according to claim 33, wherein the amplification current flowing through each of the first main leg and the second main leg is 1.2mA.

35. The operational amplifier according to claim 25, wherein a common mode output voltage is set to 1.5V.

36. The operational amplifier according to claim 25, wherein a common mode input voltage is set to 1.1V.

37. A method of processing a signal in an operational amplifier, the method comprising:
    a. amplifying the signal with a main amplifier core circuit, the main amplifier core circuit including a first main leg and a second main leg in a branch of the main amplifier core circuit;
    b. biasing the signal with a biasing circuit; and
    c. reducing power dissipation with a dynamic current switching circuit coupled to the grounded source operational amplifier circuit.

38. The method according to claim 37, wherein the main amplifier core circuit includes an upper gain enhancement circuit including a first PMOS cascode, a second PMOS cascode and an AUXP operational amplifier, further wherein the upper gain enhancement circuit maintains an upper gain bias voltage across a first PMOS current sources and a second PMOS current source.

39. The method according to claim 37, wherein the main amplifier core circuit includes a lower gain enhancement circuit including a first NMOS cascode, a second NMOS cascode and an AUXN operational amplifier, further wherein the lower gain enhancement circuit maintains a lower gain bias voltage across a main input pair.

40. The method according to claim 37, wherein the upper gain bias voltage is 500mV.

41. The method according to claim 37, wherein the lower gain bias voltage is 400mV.

42. The method according to claim 37, wherein the dynamic current switching circuit includes:

a. a main mirror diode;
b. a main fixed current source;
c. a first current switch; and
d. a second current switch.

43. The method according to claim 42, wherein when the operational amplifier circuit is in a reset state, an input signal is high, and the second current switch directs a reset current through its drain, thereby allowing none of the reset current to flow through the main mirror diode and through each of the first main leg and the second main leg.

44. The method according to claim 43, wherein the reset current flowing through each of the first main leg and the second main leg is 250uA.

45. The method according to claim 42, wherein when the operational amplifier circuit is in an amplification state, the input signal is low, and the second current switch is off, thereby allowing an amplification current to flow through the main mirrored diode, the first

current switch, the second current switch, and each of the first main leg and the second main leg.

46. The method according to claim 45, wherein the amplification current flowing through each of the first main leg and the second main leg is 1.2mA.

47. The method according to claim 37, wherein a common mode output voltage is set to 1.5V.

48. The method according to claim 37, wherein a common mode input voltage is set to 1.1V.